Four-Switch Single-Phase Common-Ground PV Inverter with Active Power Decoupling

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***Abstract*—This letter presents a transformerless single-phase PV inverter, which combines with common-ground (CG) and active power decoupling (APD) techniques. The leakage current is eliminated and bulky electrolytic capacitors are removed, thus improving the system safety and reliability. In addition, it needs only four switches and can be implemented conveniently by a commercial H-bridge module. The validity of the inverter is verified with a 2-kW prototype.**

***Index Terms*—PV inverter, grid-connected, common ground, power decoupling, leakage current.**

I. INTRODUCTION

DOUBLE-line-frequency power pulsation and leakage current problems are two critical issues in single-phase transformerless photovoltaic (PV) inverters [1].

The power pulsation is an inherent problem in single-phase systems, which affects the maximum power point tracking (MPPT) performance and shortens the lifespan of PV inverter. To buffer the pulsating power, bulky electrolytic capacitors are usually used. However, this method would degrade system reliability and power density [2]. To address these issues, the active power decoupling (APD) method has been proposed [3]. Then, long-lifetime film capacitors can be used to replace bulky electrolytic capacitors. However, in most cases, the APD method requires additional switches, which increases the cost.

The leakage current is mainly caused by the high-frequency common-mode voltage of PV inverters. Besides, studies in the last decades indicate that it also could be produced by the potential induced degradation (PID) polarization effect [4]. When the PID effect arises, the leakage current would flow through the PV frame down to the ground. For the P-type PV module, the negative ground could avoid the leakage current. Among all kinds of transformerless inverters, only the common -ground (CG) inverter could suppress the PID effect [4].

A family of CG inverters based on the switched-capacitor concept are introduced in [5], and a similar topology based on the charge-pump concept is introduced in [6]. They all feature with low leakage current, low voltage stress, and high efficiency. However, since the flying capacitor is charged directly by the voltage source, the current stress is high. Thus, their power ratings are limited. To reduce the current stress, electrolytic capacitors with high equivalent series resistance (ESR) are needed, which could reduce reliability and efficiency.

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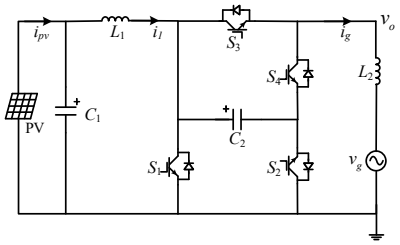


Fig. 1. Proposed transformerless PV inverter topology.

A CG inverter in [7] employs a film capacitor as the flying capacitor. The power rating is promoted to 3.7kW, but up to 9 switches and diodes are used. Several CG topologies with reduced switches and voltage-boost ability have been proposed, such as two switches in [8], three switches in [9], and four switches in [10]. All the CG inverters in [5]-[10] have no power decoupling ability, and thus bulky electrolytic capacitors are needed to buffer the power pulsation.

Two CG inverters with active power decoupling ability are introduced in [11] and [12]. Neither of them uses bulky electrolytic capacitors, and the flying capacitor currents are limited by inductors. However, the two inverters are bipolar modulated, and thus the efficiencies could be affected. A novel variable-frequency technique is proposed in [12], and the inverter has a compact structure with only two SiC switches. However, IGBT or Si MOSFET could hardly be used, since the switching frequency is up to 300 kHz and the reserved recovery problem exists in the negative half-period. Moreover, the input inductor needs to operate in discontinuous conduction mode (DCM), so this inverter can only be used at low power level.

This paper presents a single-phase CG inverter, which can be seen as an integration of the inverter in [5] with the APD method. Only four switches are needed and bulky electrolytic capacitors are replaced by film capacitors. It features with low leakage current, high reliability, and reactive power ability.

II. SYSTEM CONFIGURATION AND OPERATION PRINCIPLES

A. Proposed topology

The proposed inverter, as shown in Fig.1, consists of 4 IGBTs, 2 film capacitors, and 2 inductors. The negative terminal of PV array is grounded. Notably, the four switches

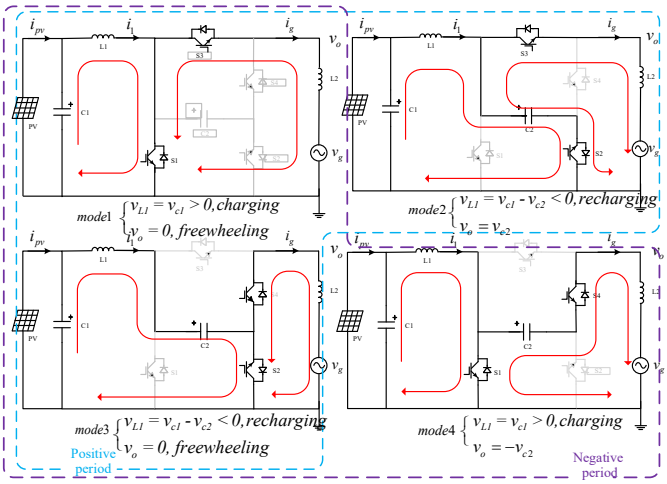
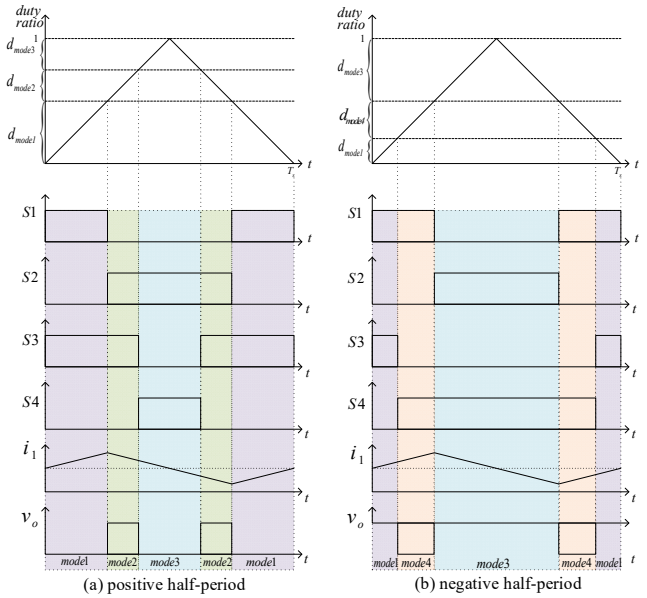


Fig. 2. Operating modes. The red arrows indicate the direction of the current.



(a) positive half-period (b) negative half-period

Fig. 3. PWM signals sequence.

compose an H-bridge, and the commercial module can be employed.

Different from the traditional full-bridge inverter, the capacitor C_2 and the inductor L_1 are added and they both play two roles. For C_2, one role is a flying capacitor, to supply negative voltage to the grid. And the other is a decoupling capacitor, to buffer the mismatch of input and output power.

For L_1, one role is to limit the current while charging C_2, and the other is to achieve power decoupling together with C_2.

B. Modulation strategy

Fig. 2 shows the four operating modes. Each half-period of the output voltage has three operation modes.

1)Positive half-period: The input inductor current rises up in mode 1 and drops down in mode 2 and 3. The output voltage v_o is equal to 0 in mode 1 and 3, and v_{C_2} in mode2.

According to the volt-second balance law, (1)-(3) should be satisfied, where d_{modeN} (N=1-4) is the duty ratio of each mode.

$$d_{mode1}v_{C_1}+(d_{mode2}+d_{mode3})(v_{C_1}-v_{C_2})=0 \quad (1)$$

$$d_{mode1}+d_{mode2}+d_{mode3}=1 \quad (2)$$

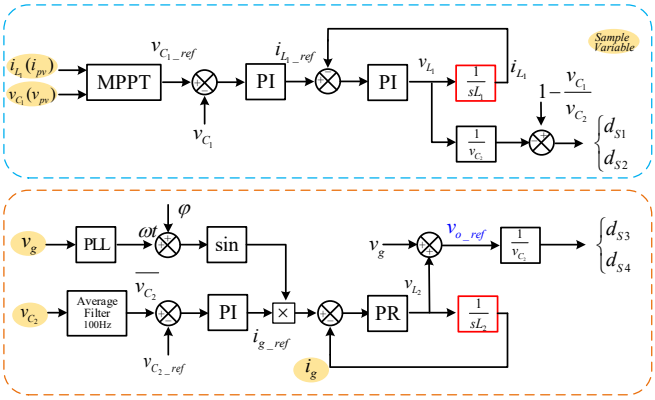


Fig. 4. Control diagram.

$$v_O=d_{mode2}v_{C_2} \quad (3)$$

The output voltage v_O can be derived as

$$v_O=d_{mode2}/(d_{mode2}+d_{mode3})v_{C_1}\le v_{C_1} \quad (4)$$

As can be seen, this inverter is a step-down type.

As seen from Fig. 2, the switch duty ratios d_{SN} (N=1-4) in positive half-period can be expressed as

$$d_{S1}=d_{mode1} \quad (5)$$

$$d_{S2}=d_{mode2}+d_{mode3} \quad (6)$$

$$d_{S3}=d_{mode1}+d_{mode2} \quad (7)$$

$$d_{S4}=d_{mode3} \quad (8)$$

Substituting (1)-(3) into (5)-(8) yields

$$d_{S1}=1-v_{C_1}/v_{C_2} \quad (9)$$

$$d_{S2}=v_{C_1}/v_{C_2} \quad (10)$$

$$d_{S3}=v_O/v_{C_2} \quad (11)$$

$$d_{S4}=1-v_O/v_{C_2} \quad (12)$$

2) Negative half-period: The input current rises up in mode 1 and 4, and drops down in mode 3. The output voltage is equal to 0 in mode 1 and 3, and $-v_{C_2}$ in mode 4. Similar to the positive half-period, (13) – (15) should be satisfied.

$$(d_{mode1}+d_{mode4})v_{C_1}+d_{mode3}(v_{C_1}-v_{C_2})=0 \quad (13)$$

$$d_{mode1}+d_{mode3}+d_{mode4}=1 \quad (14)$$

$$v_O=-d_{mode4}v_{C_2} \quad (15)$$

As seen from Fig. 2, the switch duty ratios in negative half-period can be expressed as

$$d_{S1}=d_{mode1}+d_{mode4} \quad (16)$$

$$d_{S2}=d_{mode3} \quad (17)$$

$$d_{S3}=d_{mode1} \quad (18)$$

$$d_{S4}=d_{mode3}+d_{mode4} \quad (19)$$

Substituting (13)-(15) into (16)-(19) yields

$$d_{S1}=1-v_{C_1}/v_{C_2} \quad (20)$$

$$d_{S2}=v_{C_1}/v_{C_2} \quad (21)$$

$$d_{S3}=1-(v_{C_1}+|v_O|)/v_{C_2} \quad (22)$$

$$d_{S4}=(v_{C_1}+|v_O|)/v_{C_2} \quad (23)$$

From (9)-(12) and (20)-(23), it can be seen that there're two pairs of independent duty ratios - (d_{S1}, d_{S2}) and (d_{S3}, d_{S4}), and each pair is complementary. (d_{S1}, d_{S2}) is used to control the input power, and (d_{S3}, d_{S4}) is used to control the output power,

which is different from the traditional full-bridge inverter with only one independent duty ratio.

According to $d_{SN} \geq 0$, (24) can be derived from (22).

$$v_{C_2} \geq v_{C_1} + |v_O| \tag{24}$$

According to (4), (24), the modulation index m is derived as

$$m = v_O / v_{C_2} \leq 0.5 \tag{25}$$

Fig. 3 shows the PWM signals sequence. It can be seen that all switches turn on and off once in a PWM period. S_4 in positive half-period and S_2, S_3 in negative half-period could turn off because the current flows through the antiparallel diode.

C. Control method

To obtain the duty ratios, two dual closed-loop controls are adopted, as shown in Fig. 4. In the first loop, two PI controllers work along with MPPT module to control the input power. The second loop is to control the grid current. While the input power is controlled as a constant value and the output current is controlled to be in phase with the grid voltage, C_2 is forced to buffer the mismatch of the input and output power, therefore the APD method is achieved [3].

III. System Analysis and Comparison

A. Voltage stress

According to the operating modes shown in Fig.2, it can be seen that the voltage stresses of the four switches are v_{C2}.

Assume that the grid voltage and current are given in (26), then the output power can be derived as (27).

$$v_g = V_g sin(\omega t); \quad i_g = I_g sin(\omega t + \varphi) \tag{26}$$

$$p_g = v_g i_g = \underbrace{\frac{1}{2} V_g I_g cos\varphi}_{\overline{p_g}} \underbrace{- \frac{1}{2} V_g I_g cos(2\omega t + \varphi)}_{\widetilde{p_g}} \tag{27}$$

where V_g and I_g are the magnitudes of grid voltage and current respectively, φ is power factor angle, $\overline{p_g}$ is the active power, and $\widetilde{p_g}$ is the ripple power at the double-line frequency (2ω).

Suppose all the ripple power is buffered by C_2, then its voltage can be calculated as [2]

$$v_{C_2} = \sqrt{\overline{v}_{C_2}^2 - \frac{V_g I_g}{2C_2\omega} sin(2\omega t + \varphi)} \tag{28}$$

where $\overline{v}_{C_2}$ is the average value of v_{C_2} and usually regarded as a constant in the traditional APD method [3]. Considering high v_{C_2} would lead to high voltage stress and high power dissipations, v_{C_2} should be optimally designed as follows.

According to (24) and (28), $\overline{v}_{C_2}^2$ should be constrained as

$$\overline{v}_{C_2}^2 \geq (v_{pv} + V_g)^2 + \frac{V_g I_g}{2C_2\omega} sin(2\omega t + \varphi) \tag{29}$$

To satisfy (29) all the time, the minimal average-voltage of C_2 can be expressed as

$$\overline{v}_{C_2} = \sqrt{(v_{pv} + V_g)^2 + \frac{V_g I_g}{2C_2\omega}} \tag{30}$$

It should be noted that $\overline{v}_{C_2}$ varies dynamically with the input voltage and power, and always keeps to a minimum value.

The optimal voltage stress of four switches can be derived from (28) and (30) as

TABLE I
System Parameters

Parameters	Value	Parameters	Value
Input voltage	180 V	Capacitor (C_1)	40 μF, 400 V
Grid voltage	110 Vrms	Capacitor (C_2)	100 μF, 600 V
IGBT	FGA40N65SMD	Inductor (L_1)	3 mH
Switching frequency	20 kHz	Inductor (L_2)	2.2 mH

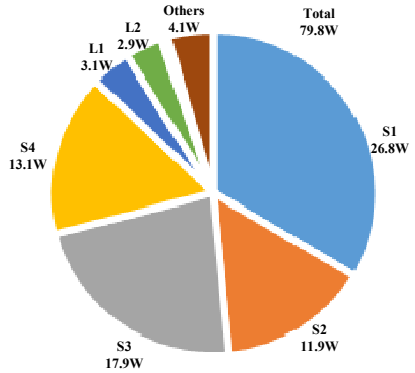


Fig. 5 Power losses at 2-kW.

$$v_{max} = \sqrt{(v_{pv} + V_g)^2 + \frac{V_g I_g}{C_2\omega}} \tag{31}$$

B. Current stress

As seen from Fig. 2, the switch S_1 and S_2 in negative half-period suffer from the same maximum current stress, which can be expressed as

$$i_{max} = i_{L_1} + I_g \tag{32}$$

where, i_{L_1} is the input inductor current, and I_g is the peak amplitude of grid current.

The currents of S_3 and S_4 are always the same as grid current, so their current stresses can be expressed as

$$i_{S3} = i_{S4} = I_g \tag{33}$$

C. Design of components

The inductor L_1 works like a boost inductor, and its inductance can be calculated as [13]

$$L_1 = \frac{v_{C_1}}{\lambda_{L_1} \overline{i}_{L_1} f_{sw}} (1 - \frac{v_{C_1}}{v_{C_2}}) \tag{34}$$

where $\overline{i}_{L_1}$ is the average current of L_1, λ_{L_1} is the allowable current ripple ratio of L_1, and f_{sw} is the switching frequency.

The inductor L_2 is used as an output filter, and its inductance can be calculated as

$$L_2 = \frac{v_g}{\lambda_{L_2} \overline{i}_{L_2} f_{sw}} (1 - \frac{v_g}{v_{C_2}}) \tag{35}$$

where $\overline{i}_{L_2}$ is the average current of L_2, and λ_{L_2} is the allowable current ripple ratio of L_2.

The capacitor C_1 is used as an input filter, buffering the current ripple of L_1. Its capacitance can be calculated as

$$C_1 \geq \frac{\lambda_{L_1} p_{pv}}{\lambda_{C_1} v_{C_1}^2 f_{sw}} \tag{36}$$

where p_{pv} is the PV power, and λ_{C_1} is the allowable voltage ripple ratio of C_1.

TABLE II
COMPARISON OF THE PROPOSED INVERTER

Inverters	[5] (Type I)	[6]	[7]	[8]	[9]	[10]	[11]	[12]	Proposed
Power decoupling	No	No	No	No	No	No	Yes	Yes	Yes
Unipolar modulation	Yes	Yes	Yes	No	No	No	No	No	Yes
Switches No.	4	4	6	2	3	4	4	2	4
Switch Voltage(V)	1200	1200	1200	1200	600	300	1200	None	650
Capacitors	2	3	2	2	2	2	2	3	2
Capacitor Voltage(V)	400	500	None	None	None	None	1100	None	600
Diodes	1	2	3	0	0	0	0	1	0
Inductors	1	1	2	2	2	2	2	3	2
Voltage stress	Vin	Vin	Vin	Vin+Vg	1.6Vg	Vin+Vg	>Vin+Vg	5Vg	3Vg
Grid Voltage(V)	230	220	230	110	110	110	240	70	110
Power rating (kW)	1	0.5	3.7	0.2	0.28	0.3	3	0.18	2
Switch type	SiC	SiC	Si	SiC	Si	MOSFET	SiC	SiC	Si
Switching frequency(kHz)	20	24	12	40	40	50	75	20-300	20
Efficiency (%)	99.2	97.4	97	96	93	95.7	96.4	96.4	96.5

The flying capacitor C_2 is used to buffer the mismatch of the PV power and grid power. Its capacitance can be calculated as

$$C_2 \geq \frac{2p_{pv}}{[v_{CE}^2 - (v_{pv}+V_g)^2]\omega} \tag{37}$$

where v_{CE} is the maximum voltage of switches, and ω is the line frequency.

The nominal condition can be designed as p_{pv}=2kW, v_{C_1}=180V, f_{sw}=20kHz, λ_{L_1}=20%, λ_{L_2}=15%, λ_{C_1} =2%, v_{CE}=650V, ω=100π. Substituting the above-mentioned parameters into (34)-(37) yields $L_1 \geq$2.6mH, $L_1 \geq$2mH, $C_1 \geq 31\mu$F, $C_2 \geq 41\mu$F. Considering some margin, the selected component parameters are given in Table I.

D. Power losses

The power losses calculated by PLECS at 2kW are shown in Fig.5.

E. Comparisons with the prior-art topologies

Table II presents a comparison of the proposed inverter with other common-ground inverters. The numbers of required active and passive components are shown concisely here for comparison. It can be seen that compared with the other inverters in combination with both power decoupling function and unipolar modulation, the proposed topology requires the least switches.

IV. EXPERIMENT RESULTS

A 2-kW prototype is built to verify the feasibility of the proposed inverter, shown in Fig. 6. The DSP controller is TMS320F28335. The PV simulator is ITECH IT6018C, and the AC source is Chroma 61830.

Fig. 7(a) shows the 2-kW experimental results at unity power factor (PF). It can be seen that although the PV capacitor C_1 is only 40 μF, the PV current is kept constant, which illustrates the validity of the power decoupling method. The grid current is sinusoidal, and the total harmonic distortion (THD) is 3.3%.

Fig. 7(b) shows some key waveforms in the steady-state. The flying-capacitor voltage fluctuates per 10 ms, which is in agreement with the power decoupling method. Due to the common-ground structure, the root-mean-square (RMS) of the leakage current is only 4.16 mA. The peak current of the flying capacitor is the same as the output current, unlike the switched-capacitor suffering from impulse charging current. The output voltage shows a 3-level characteristic, which illustrates that the inverter works in the unipolar modulation mode.

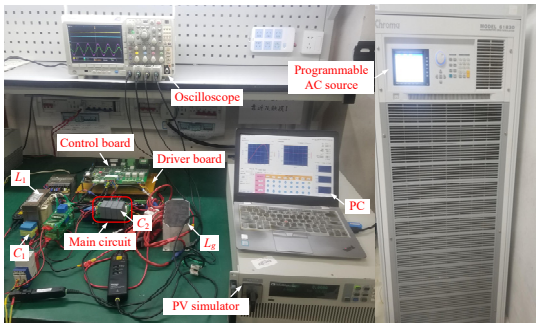


Fig. 6. The prototype picture.

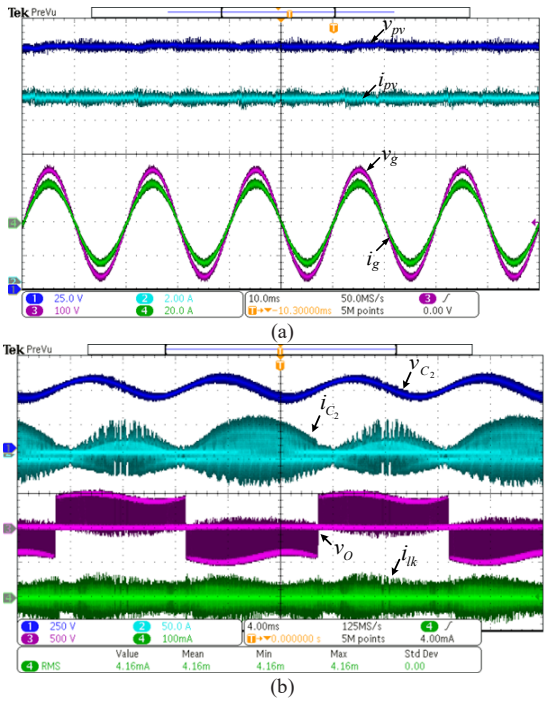


Fig. 7. Steady-state waveforms at 2-kW and unity PF. (a) input/output voltage v_{pv}, v_g and current i_{pv}, i_g, (b) flying-capacitor voltage v_{C_2}, current i_{C_2}, output voltage v_O, and leakage current i_{lk}.

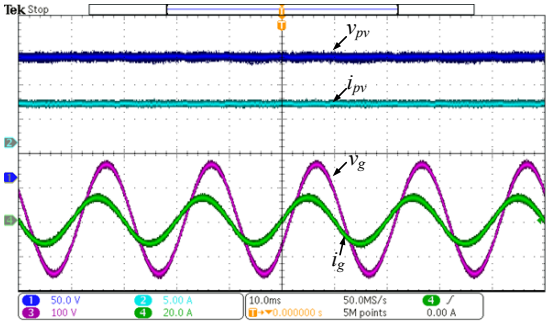


Fig. 8. Reactive power with 0.86 PF leading.

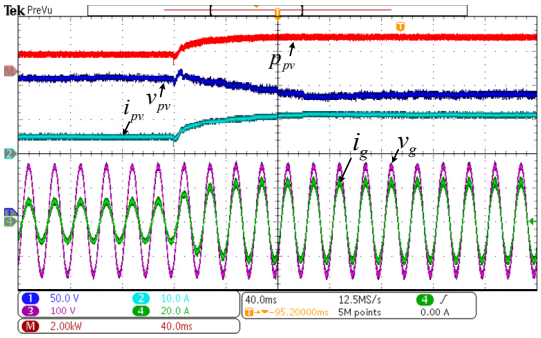


Fig. 9. Transient response of MPPT with step-up power from 1kW to 2kW.

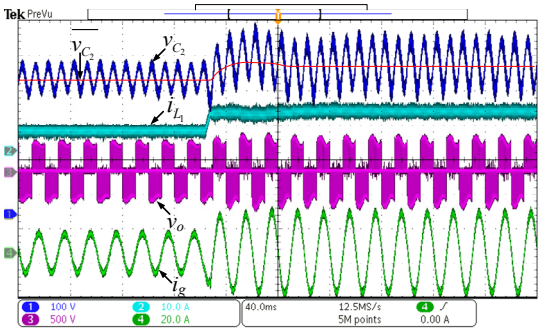


Fig. 10. Dynamic experimental results of capacitor voltage v_{C_2}.

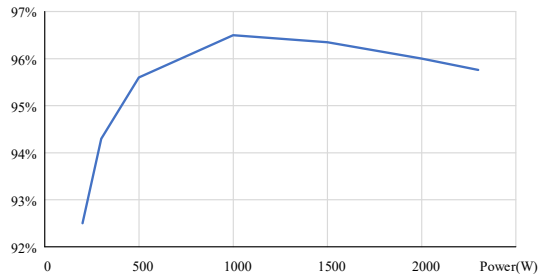


Fig. 11. Measured experimental efficiency.

Fig. 8 shows the ability to generate reactive power. And the output power factor is 0.86 leading.

The transient response of MPPT is shown in Fig.9. As can be seen that, although the PV power changes from 1kW to 2kW, the system is stable and the transient time is less than 120ms, verifying the effectiveness and good performance of the proposed topology.

Fig.10 shows the dynamic waveforms of the average voltage $\overline{v}_{C_2}$. As can be seen, when the PV power changes suddenly from half-load to full-load, the average voltage $\overline{v}_{C_2}$ increases automatically. The result is consistent with the optimal design in Part III-Eq.(30). Thus, the voltage stress of switches will always be kept at the minimum value dynamically, which is beneficial to improve the system efficiency.

The measured efficiency curve of the proposed inverter is shown in Fig.11. The peak efficiency is 96.5% and is close to the prior-art topologies. Additionally, the efficiency can be improved by using wide bandgap switches.

I. Conclusion

This letter presents a transformerless single-phase PV inverter. A 2-kW prototype has been built and evaluated. It benefits with several advantages:

1) It has a common-ground structure, and the experimental leakage current is only 4.16 mA;

2) It utilizes the active power decoupling method, and total film capacitors of 140 μF are used instead of bulky electrolytic capacitors, which increases the system reliability and lifetime;

3) Only four switches are used and the commercial H-bridge module can be employed.

Thus, the presented converter offers a promising solution for the PV power generation system.

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